Thesis M.Sc.

IDP

Automated Performance Analysis of an FPGA-based P4 Platform

Motivation

P4 [1] is a programming language intended to describe the behavior of packet processing systems. P4 was introduced in 2014 and can be used to define entirely new networks with new protocols which behave differently from the networks we currently use. The main focus for usage is to implement switching and routing capabilities.

P4 programming language

One of the available P4-enabled devices is the NetFPGA SUME platform [2]. This FPGA, usually programmed using a hardware description language (HDL), can be programmed using the P4 language.

In a previous work we have developed a test framework for P4 devices, similar to Whippersnapper [3]. It analyses basic components of the P4 language (parser, modifying header fields, . . .) by performing automated and standardized peformance measurements. We have since then applied the framework to the NetFPGA platform.

The goal of this thesis is to continue this work by extending and improving the framework. For instance, more language features can be analysed. Furthermore, a newer P4 to VHDL compiler version can be used.

Tasks

- Get familiar with the P4 language and NetFPGA platform
- Get familiar with our current framework
- Extend the framework
- Run reproducible performance measurements
- Model the behavior of the NetFPGA platform

The framework is written using python and ansible. FPGA programming knowledge is NOT required.

Sources

- [1] https://p4.org/
- [2] NetFPGA SUME: Toward 100 Gbps as Research Commodity, Zilberman et al., 2014
- [3] Whippersnapper: A P4 Language Benchmark Suite, Dang et al., 2017

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